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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/473,305	12/28/99	FRUTSCHY K	42390-P7663

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PAREKH, N	
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ROBERT G WINKLE INTEL CORP
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 WILSHIRE BLVD
7TH FLOOR
LOS ANGELES CA 90025

DATE MAILED: 06/21/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary

Application No.	Applicant(s)
09/473,305	Frutschy et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 24, 2001*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 2, 4-7, 12-16, 23, 25, and 28-33* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 2, 4-7, 12-16, 23, 25, and 28-33* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 9

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4-7 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (US Pat. 5783461) in view of Hembree et al (US Pat. 5931685) and Domadia et al (US Pat. 5949137).

Regarding claim 1, Hembree discloses a microelectronic component assembly comprising:

- a first substrate having a first and second surface and the first surface including contacts (microelectronic device substrate 12, Fig. 2)

- an interposer substrate having a first and second surface and the first surface including contacts (interposer substrate 16, Fig. 2)

- microbumps/solder balls extending between the first substrate and an interposer substrate contacts where the microbumps/solder balls are attached to the interposer substrate contact (bumps 60B-Fig. 5A; Fig. 4-6; Col. 6, line 21- 65), and

- a compression mechanism/support structure for imparting pressure between the first substrate and second substrate (18 and 26 in Fig. 1 and 2; Col. 3, line 35)

(Fig. 1-10; Col. 1, line 55- Col. 6, line 65).

Hembree fails to specify using microbumps/solder balls attached to the substrate/first substrate contact and the interposer substrate being a motherboard. However, it is conventional in the chip interconnection technology art to attach the solder balls/bumps on any substrate such as die, carrier, interposer, etc. and to incorporate an interposer/carrier substrates such as expansion card, motherboard, MCM card, etc. to achieve the interconnection, testing and design requirements. The cited reference by Farnworth et al teach using solder ball placement interchangeably on die or carrier substrate (Col. 4, line 10) to meet the interconnection requirements. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate solder balls attached to the second substrate contact and designate the interposer substrate being a motherboard to achieve the electrical testing and design requirements in Hembree's assembly as cited in claim 1.

Regarding claims 2 and 4, Hembree discloses the substrate/first substrate comprising a microelectronic package/carrier substrate/microelectronic device (Fig. 2; Col. 1, line 55- Col. 4, line 47).

Regarding claim 5, Hembree discloses an interposer substrate/motherboard contact/non-reflow electrical contact comprising a recess defined by sidewalls (vertical and inclined) extending into second substrate and conductive material layered in the recess (Fig. 5 and 5A; Col. 6, line 34-65).

Regarding claims 6 and 7, Hembree fails to specify the dimensions such as a width and shape of the interposer substrate/motherboard contact being same as a diameter of the solder ball and shape of a semispherical surface of same radius as that of the solder ball respectively. Hembree et al teach forming non-reflow solder ball contact comprising a recess defined by vertical sidewalls (40 in Fig. 3; Col. 5, line 40; Col. 5-8) extending into the substrate (26 in Fig. 3) and conductive material (42 in Fig. 3) layered in the recess (Fig. 3-3E; Fig. 6A-10A). Hembree et al further teach selecting the size, shape (circular, oval, square, etc.), dimensions, etc. of the recess including the conductive material (40 /42 in Fig. 3) and diameter of the bump/ball such that the electrical contact within the recess can be accomplished to compensate for the variation in the in the diameter/shape of the bump/ball with minimal bump deformation (Col. 5, line 39-66). Fig. 10A in Hembree et al shows the recess (Fig. 10A) where the width of the recess is substantially same as a diameter of the solder ball and the void is formed in the recess (Col. 9, line 30). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to select the dimensions such as width/shape of the interposer substrate/motherboard contact being same as a diameter of the solder ball and shape of a semispherical surface of same radius

as that of the solder ball to to improve the electrical contacting within the recess using Hembree et al's recess structure in Hembree's assembly.

Claim 29-31 are rejected as explained above for claims 1; 5-7 respectively.

3. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (US Pat. 5783461) in view of Hembree et al (US Pat. 5931685) Domadia et al (US Pat. 5949137).

The teachings of Hembree, Hembree et al and Domadia et al apply to Claim 12 as explained above for claims 1 and 5.

Regarding claims 13 and 14, Hembree discloses compression mechanism/support structure comprising:

- a frame portion (portion 36 in Fig. 2) of the base
- a backing plate/strip (strip 31 in Fig. 2) abutting the second surface second surface
- a cover plate/thermal plate (plate 24 in Fig. 2) extending over the frame portion and adjacent to the first substrate
- a resilient elastomeric spacer ring/washer spring (washer 22 in Fig. 2) extending between the thermal plate and the microelectronic device/interposer substrate, and
- plurality of retention devices such as clips and clamps

(Fig. 1-10; Col. 1, line 55- Col. 6, line 65).

Hembree fails to specify the retention devices comprising a plurality of bolts and nuts extending through the backing plate, frame and thermal plate. Domadia et al teach using a support structure where the plurality of retention devices having a plurality of bolts and nuts extending through the back of the substrate, stiffener/frame portion and thermal plate/heat dissipater (Fig. 5-7; Col. 4, line 40-Col. 6, line 48). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the retention devices comprising a plurality of bolts and nuts extend extending through the backing plate, frame and thermal plate to reduce the mechanical stress on the device using Domadia et al's retention device Hembree's assembly as cited in claims 13 and 14.

Regarding claim 15, Hembree discloses the first substrate comprising a microelectronic device package including a microelectronic device attached to and in electrical contact with a first surface of an interposer/multilayered TAB tape with multilayer contact surfaces where the first substrate first contact comprises contacts on a second surface of the interposer substrate (Fig. 2-5A; Col. 6, line 21- Col. 6, line 65; Col. 1, line 55- Col. 4, line 47).

Claim 16 is rejected as explained above for claims 12-14.

4. Claims 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (US Pat. 5783461) in view of Hembree et al (US Pat. 5931685) and Domadia et al (US Pat. 5949137).

Regarding claim 23, as explained above for claims 1 and 5, Hembree discloses an interposer substrate/motherboard contact/non-reflow electrical contact comprising a recess defined by sidewalls extending into second substrate and conductive material layered in the recess (Fig. 5 and 5A; Col. 6, line 34-65) but fails to specify the conductive material layered on the vertical sidewall. Hembree et al teach forming non-reflow solder ball contact comprising a recess defined by vertical sidewalls (40 in Fig. 3; Col. 5, line 40; Col. 5-8) extending into the substrate (26 in Fig. 3) and conductive material (42 in Fig. 3) layered in the recess (Fig. 3-3E; Fig. 6A-10A). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate a recess defined by vertical sidewalls extending into the substrate and conductive material layered on the vertical sidewall in the recess to improve the electrical contacting the recess using Hembree et al's recess structure in Hembree's substrate.

Regarding claim 25, Hembree fails to specify the dimensions such as a width and shape of the recess including the conductive material being same as a diameter of the solder ball. As explained above for claim 23, Hembree et al further teach selecting the size, shape (circular, hemispherical, square, etc.), dimensions, etc. of the recess including the conductive material

(40 /42 in Fig. 3) and diameter of the bump/ball such that the electrical contact within the recess can be accomplished to compensate for the variation in the in the diameter/shape of the bump/ball with minimal bump deformation (Col. 5, line 39-66). Furthermore, Hembree et al teach using the recess where the width of the recess is substantially same as a diameter of the solder ball and the void is formed in the recess (Fig. 10A; Col. 9, line 30). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to select the dimensions such as a width/shape of the recess including the conductive material being same as a diameter of the solder ball to improve the electrical contacting the recess using Hembree et al's recess structure in Hembree's substrate.

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (US Pat. 5783461) in view of Hembree et al (US Pat. 5931685) and Domadia et al (US Pat. 5949137).

Claim 28 is rejected as explained above for claims 1, 5-7 and 23.

6. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (US Pat. 5783461) in view of Hembree et al (US Pat. 5931685) and Domadia et al (US Pat. 5949137).

Claim 32 is rejected as explained above for claims 1, 5-7 and 23.

Regarding claim 33, as explained above for claims 32, 1, 5-7 and 23, Hembree fails to specify using a resilient material disposed between the substrate and the conductive material layer. Hembree et al teach using conventional resilient/elastomeric material (48 in Fig. D.) disposed between the substrate and the conductive material layer to improve the cushion effect for the substrate contact (Col. 8, line 15-34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a resilient material disposed between the substrate and the conductive material layer to improve the cushion effect for the substrate contact using Hembree et al's recess structure in Hembree's assembly.

Papers related to this application may be submitted directly to Art Unit 2811 by Facsimile transmission. Papers should be faxed to Art Unit via Tech Center 2800 fax center located in Crystal Plaza 4, Room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh at (703) 305-3410. The examiner can normally be reached on Monday-Friday from 08:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

06-17-01

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER